A Two-Stage Interleaved Bridgeless SEPIC based PFC Converter for Electric Vehicle Charging Application

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***Abstract*— Electric vehicles are become more popular nowadays due to negligible gas emissions and less dependent on fossil fuel. However, the battery charging process is the main challenge that influences the electric vehicle (EV) transportation system. The power factor correction (PFC) and dc-dc converter stages are the main phases in the EV charging system. Various electric vehicle charging technologies are developed using different power electronics converter topologies, such as cuck, Zeta, SEPIC, and buck-boost converter. SEPIC (Single Ended Primary Inductor Converter) converter topology is the most preferred topology for battery charging applications due to providing non-inverting output with buck boost operation and reduced input and output ripple current. Although the SEPIC convertor topology has many advantages still possess a lot of challenges. The main challenges are reducing the converter size, conduction loss, voltage stress and increasing the efficiency when compared with the existing recent developed Bridgeless SEPIC topologies with interleaved concept. In this proposed research, a modified interleaved bridgeless, SEPIC based converter is proposed to improve the Power Quality (PQ) for vehicle charging station. The proposed topology is able to reduce the voltage stress, power loss, increase the converter efficiency and improve the power factor due to the bridgeless with interleaved configuration compared to other topologies. The preliminary design of the of the bridgeless interleaved topology is developed with the help of MATLAB Simulink software. The various preliminary results were obtained at the input supply voltage of 70 – 230 V ac supply.**

Keywords—SEPIC converter, battery charger, PFC converter, CUK converter, boost converter

I. INTRODUCTION

Due to the increasing effect of carbon dioxide emissions, greenhouse effect and the reduction of fossil fuel the transportation industry forced to produce more electric vehicles alternatively to the internal combustion engine. In the last few years, the production of plug-in electric vehicles PEVs) are increasing due to the awareness of sustainable energy, improvement in battery technology and lowering in cost of PEVs [1]. According to the Electric Vehicle (EV) world sales database, even though the business sector is far away in 2021, EV sales reached the highest level. From January to June 2021, the deliveries have increased by 1,66 million units compared to 2020 [2]. A good charging infrastructure able to provide the required energy demand with appropriate controlled charging speed and compensate the driving range issues [3]. The main purpose is to supply the electrical power for charging the battery in the electric vehicle [4]. There are two different types of charger stations they are; on-board and off-board charger. Both types are suitable for unidirectional or bidirectional power flow. The power handling capability of an on-board charger is lower and limited by space, weight and cost [5]. The off-board charger is designed to carry more kilowatts of power and reduce the substantial weight of the Plug in Hybrid Electric Vehicle (PHEV). Generally, the charging system can be classified in to two types. They are; AC and DC charging systems [4].

The charging system has different charging levels, namely, level 1 (residential charger with single phase AC supply), level 2 (commercial charger with single or three phase AC supply) and level 3 (fast charger with three phase AC or DC supply). Level 1 and level 2 charging systems are mostly used for on-board charging applications and take longer time for charging. However, the level 3 charging system takes short time for charging the battery and, used for off-board charging applications [6] [7]. The utility current drawn from the EV charger must be with low distortion to reduce the power quality impact and improve the power factor to take the full advantages of real power accessible from a utility port [5]. An EV charging architecture consists of a PFC stage and a dc/dc converter stage [8]. The controller circuit is necessary to control the operation of the PFC stage, dc-dc converter stage and vehicle communication stage. The charger size and efficiency is depending upon the structure and number of components of a dc-dc converter [9]. The increased usage of uncontrolled rectifiers, variable speed drives and other power semiconductor switching devices affects the

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power quality of the utility system and generates the harmonics more than the value specified by the International Electro Technical commission (IEC) 61000-3-2 standards [10). The more harmonics in the grid current reduce the unity power factor operation [9]. The PFC is mainly used in ac-dc converter to shape the input current more sinusoidal [11]. The PFC for the battery charger should be designed to meet the IEC 61000-3-2 standard in which the current flowing through the line should follow exactly the line voltage, the Total Harmonics Distortion (THD) should be less than 5% and the power factor is unity [12]. In traditional converter, buck or boost type PFC converter with less number of components used to minimize the power quality issues [13]. However, the buck-boost topologies provide an effective charging with wide duty cycle range, when the sudden change of fluctuating line voltage occurs [14]. A review on single phase improved ac-dc converter [15] such as Cuk, Zeta, fly back and Single-ended primary-inductance (SEPIC) converters are discussed to demonstrate the power quality operation. The Cuk based PFC converter has the benefits of low ripples at the input and output. However, for high power applications, the Cuk converters need high current rating series capacitor [16]. The Zeta based PFC converter is not appropriate in EV charger because of the bulky filter needed to reduce the ripple current at the input [17]. The SEPIC converter has an attractive solution for EV charger due to having buck and boost function with positive output voltage and low input ripple current. Due to low harmonics at the input terminal of the SEPIC converter, it does not need any additional bulk filters [12]. When compared to Cuk converter the Zeta and SEPIC converters offers small capacitor with high power density [18].

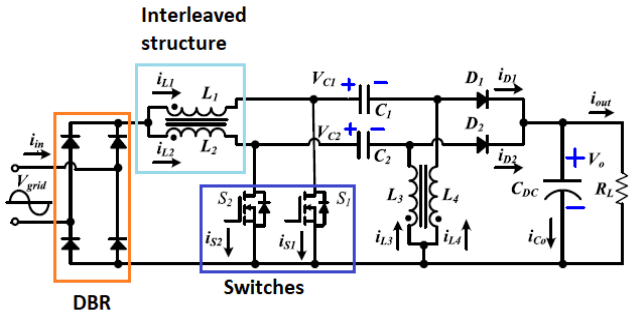

Fig.1: Conventional Interleaved SEPIC PFC converter [20]

The PFC based SEPIC converts has a disadvantage due to the high current stress across the output capacitor, which produces high voltage stress across the switches [12]. The Isolated SEPIC DC–DC Converter has been designed to achieve the high voltage gain by using the isolation transformer [19]. However, the transformer leakage reactance introduces large switch voltage due to the voltage spikes during the turn-off period. In Fig.1 the interleaved two-phase SEPIC based PFC has proposed [20] to reduce the number of magnetic components and decrease the input ripple current. But the THD is higher at lower output power and less at high output power. The large coupled inductor and bridge diode rectifier is used, this increases the size and number of components. A bridgeless isolated SEPIC converter for PFC based EV battery charger is presented in [21] to reduce the conduction losses. Furthermore, the presented converter required the bulky input inductor to reduce the harmonics current at the input, and this increases the system size. The Development of a three-phase interleaved converter based on SEPIC presented operating in dis-continuous conduction mode. The proposed scheme ensures the reduction of stresses on the semiconductor switches because of power divided over the interleaved modules. The same researcher developed the experimental prototype as shown in Fig.2 for single phase, 4 kW, interleaved SEPIC module, which shows unity power factor and the THD of 4.22% [8].

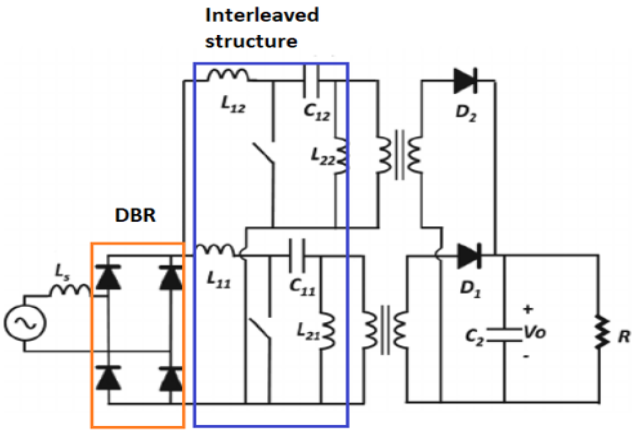

Fig.2. Conventional Interleaved SEPIC converter [8]

However, the presented converter has power loss due to the bridge type converter at the input, and the size of the converter module is bulky. At present, the SEPIC based PFC have demonstrated superiority over the other type of PFC topology to charge the EV. Despite having numerous advantages, there are challenges to design the appropriate PFC converter for the EV charger. The power quality of the PFC is important in EV charger to reduce the THD and improve the power factor. The reduced number of components are significant for the better efficiency. The lower voltage and current stresses in the switching devices are vital to improve the power level. In this research an interleaved bridgeless SEPIC based two-stage, two phase PFC is proposed to satisfy the above mentioned criteria.

II. PROPOSED TWO-STAGE, TWO PHASE INTERLEAVED SEPIC CONVERTER

Different EV charging PFC topologies have various advantages and disadvantages. Most of the PFC converters topologies emphasis on the improvement of power quality and reliability of the converter. From the literature study, each topology such as, Cuk, Zeta, ZEPIC and Boost converter implemented with a different configuration to improve the power quality and system reliability. Among the all type of topology mentioned above, the SEPIC converter is the most suitable type of converter to improve the power quality in PFC for charging EV. Most of the recent SEPIC converter configuration is designed with bridgeless PFC for charging EV battery. The bridge-less configuration is capable to mitigate the conduction losses introduced by the ac- dc bridge rectifier circuit, thus increases the conversion efficiency of the PFC based EV charger. Some PFC based SEPIC converter designed with the diode bridge rectifier followed by the interleaving single stage configuration. The interleaving converter configuration able to reduce the input and output ripple of the PFC based converter, thus reduce the voltage ripple. In order to reduce the conduction losses and improve the power quality, the bridgeless interleaved circuit with two blocks, two phase configuration is introduced at the PFC stage of the EV charger based on SEPIC topology. The proposed topology is to reduce the input and output current ripples of

the PFC converter. The proposed topology is designed with two power semi-conductor switches to reduce the components count compared to conventional SEPIC design to improve the overall efficiency.

III. Circuit Operation of Proposed SEPIC Converter

The proposed two-stage, two phase bridgeless interleaved SEPIC based PFC converter is shown in Fig.3. The proposed topology is designed with two interleaved SEPIC converters connected in parallel to process the power during each switching cycle. The circuit has one MOSFET switch (S_1 and S_2) in each phase of the converter to reduce the component count. The diodes D_5 and D_6 are used to connect the input ac voltage to the ground and reduces the noise due to the EMI. The operation of the proposed converter works in positive and negative cycles of input ac supply.

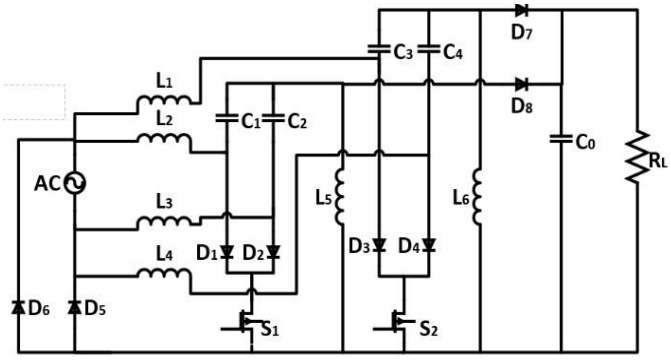

Fig. 3. Proposed two-stage, two phase bridgeless interleaved SEPIC based PFC converter

The phase 1 of the converter group consists of input inductor L_2, L_3, the capacitor C_1, C_2, the diode D_1, D_2 the semiconductor switch S_1 and the output inductor L_5. The input inductor L_1, L_4, the capacitor C_3, C_4, the diode D_3, D_4 the semiconductor switch S_2 and the output inductor L_6 are the components in phase 2. The capacitor C_0 is the output dc link capacitor commonly connected for phase 1 and 2. The operation of the proposed converter can be explained with four (4) modes of operation.

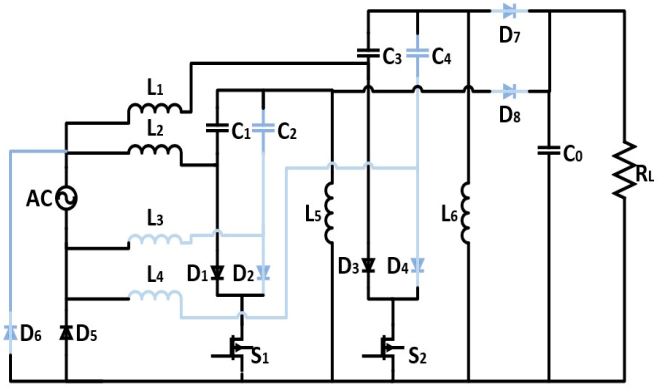

Fig. 4. Mode-1 (Positive half cycle with switch S_1 and S_2 ON)

A. Mode-1 (positive half cycle with S_1 and S_2 ON):

During the positive cycle of input ac voltage, the switch S1 and S2 will be turned ON as shown in Fig. 4. The voltage across the inductor L_1 charges in the positive side and L_2 in the negative side. Diode D_1 and D_3 become forward biased and the capacitor C_1 and C_3 will be charged. Due to the voltage across the inductor L_5 and L_6 reverses the diode D_7 and D_8 will be reverse biased.

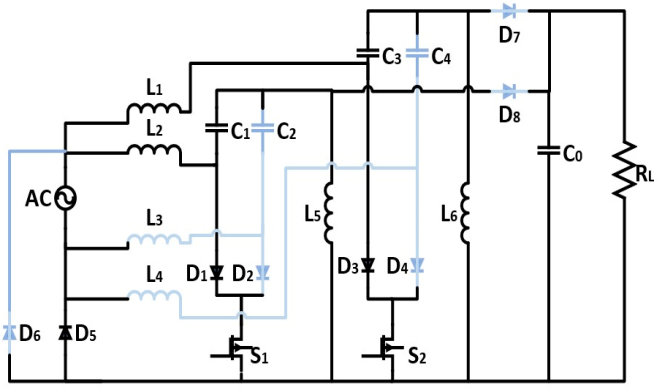

Fig. 4. Mode-1 (Positive half cycle with switch S_1 and S_2 ON)

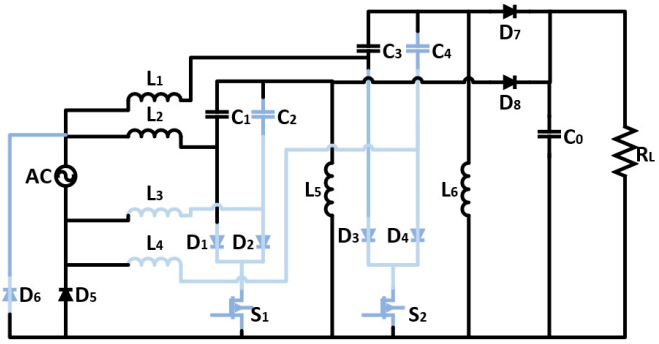

Fig.5. Mode-2 (Positive half cycle with switch S_1 and S_2 OFF)

B. Mode-2 (Positive half cycle with S_1 and S_2 OFF)

When the inductor L_1 and L_2 charges in the positive half cycle the switches S_1 and S_2 will be turned OFF as in Fig.5. The diode D_7 and D_8 will be forward biased, so the voltage will be appeared at the output. When the switch S_1 and S_2 turned OFF the diode D_1 and D_3 also will be turned OFF. The D_5 will be ON in mode 1 and 2 for the return path.

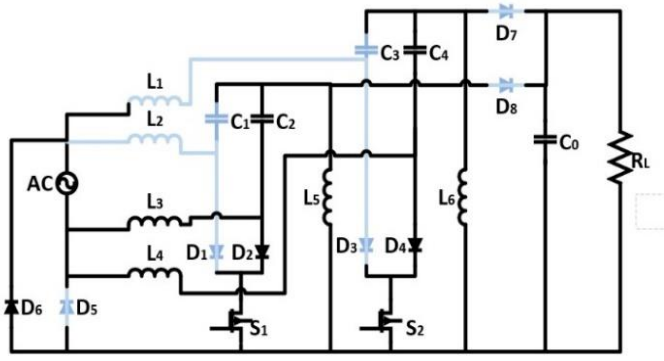

Fig.6. Mode-3 (Negative half cycle with switch S_1 and S_2 ON)

C. Mode-3 (Negative half cycle with S_1 and S_2 ON)

During the negative half cycle, the switch S_1 and S_2 will be turned ON as shown in Fig. 6. The inductor L_3 and L_4 will be charged in the negative cycle. The switch S_1 and S_2 will be turned ON with the diode D_2 and D_4. The capacitor C_1 and C_2 will be OFF and the diode D_7 and D_8 will be reveres biased thus produces no voltage at the output

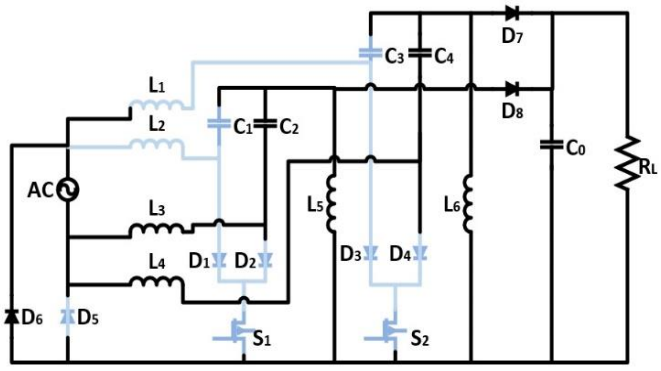

Fig.7. Mode-4 (Negative half cycle with switch S_1 and S_2 OFF)

D. Mode-4 (Negative cycle with S_1 and S_2 OFF)

The switch S_1 and S_2 will be turned OFF when the inductor L_3 and L_4 starts dis-charged as in Fig.7. The diode D_7 and D_8 become forward biased and provide the voltage at the output through the dc link capacitor C_0.

IV. DESIGN OF CIRCUIT COMPONENTS FOR PROPOSED SEPIC CONVERTER

Table 1 shows the circuit specifications for the proposed converter. Based on the mode of operation the passive components are designed for the charger operation

TABLE I. DESIGN PARAMETERS

Parameters	***Values***
Input inductor (L1, L2, L3 and L4)	1200 µH
Input capacitor (C1, C2, C3 & C4)	0.5 µF
Inductor (L5 and L6)	1.2 H
Output capacitor (C0)	500 µF
Input voltage	70-230 Vrms
Output voltage	100-320 V

A. Determining the input inductor

The input inductors in positive and negative cycles of the converter can be determined by using (1).

$$L_1 = L_2 = \frac{V_{AC}(t) \cdot D}{\Delta I_{LX} \cdot f_s} \quad (1)$$

Where,

D is the duty ratio

ΔILx is input current ripple

The input current ripple can be calculated with the help of peak input current value as shown in (2).

Where,

P_0 is the output power

η is the efficiency of the converter and

V_1 is the input supply voltage

$$I_1 = \frac{2 \times P_0}{\eta \times V_1} \quad (2)$$

The duty ratio can be calculated from (3)

Where,

V_0 is the output voltage of the converter

$$D \leq \frac{V_0}{V_1 I_1} \quad (3)$$

B. Determining the output inductor

The output inductor can be calculated by using (4).

$$L_0 = \frac{2L_x . L_e}{L_x - L_e} \quad (4)$$

Where

L_0 is the output inductance

The equivalent inductance (Le) can be calculated from (5).

$$L_e = \frac{k_e . R_L}{2 . f_s} \quad (5)$$

Where

fs is the supply frequency

R_L is the load resistance

The value of ke should be less than ke-critical to ensure the charger operation

$$k_e = 0.85 \times k_{e\text{-}cri} \quad (6)$$

$$k_{e\text{-}cri} = \frac{1}{2(M+2)^2} \quad (7)$$

The voltage conversion ratio (M) can be calculated form

$$M = \frac{V_0}{\sqrt{2} . V_{AC}} \quad (8)$$

C. Determining the output capacitor

The input capacitance required to design with appropriate value to avoid the low frequency oscillation. The value of energy transfer input capacitance designed based on the input and output inductance. For the better approximation, the resonant frequency can be calculated from expression (9).

$$f_r = \frac{1}{2\pi\sqrt{C_x(L_x + L_0)}} \quad (9)$$

The output capacitance required to obtain the desired output ripple can be expressed as below in (10)

$$C_0 = \frac{P_0}{V_0 \times \Delta V_0 \times 4 \times f_{ac}} \quad (10)$$

Several condition need to be considered to design the appropriate value of passive components to avoid any additional energy transfer.

V. RESULTS AND DISCUSSIONS

A two-stage, two phase inter-leaved bridgeless SEPIC converter operation has been simulated in MATLAB simulation software. Prospective result has been found with the simulation parameters mentioned in Table 1 being applied. Fig.8 shows the input voltage, output voltage and current waveform for the proposed converter at 230 V ac input supply. When the supply voltage is 70 V the output voltage is 96.25 V dc. At 230 V ac input the voltage measured at the output is 220 V dc. When the supply voltage is 230 V

the power factor measure is 0.9938. This high value of power factor represents the voltage stress in the switching devices are low and thus reduces the current stress in the devices as well as the passive components will be lower. When the voltage and the current stress in the converter decreases the power loss in the converter will be decreases, thus will increase the efficiency of the converter.

Fig.9 shows the voltage across the input and the inductor waveforms. The voltage across inductor 1 and 2 referred to the phase 1 operation of the converter. When the cycle is positive the inductor L_1 and L_2 will charge and discharge during cycle of operation. The diode D_1, D_3, S_1 and S_2 will conduct when the inductor charges and the voltage across the inductor rises. The voltage across the inductor L_1, L_2 and L_3 has slightly lower ripple content compared to other topology.

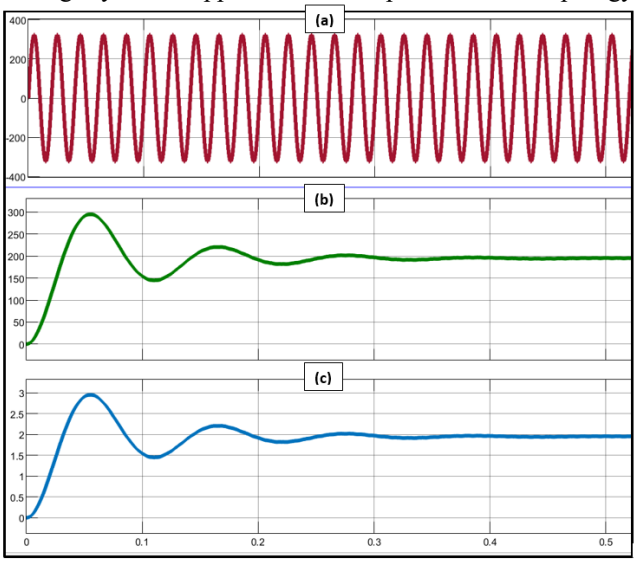

Fig.8. Performance of the converter at the input and output. (a) voltage across the input at 230 V (rms). (b) voltage across the output at 220 V dc, and (C) Output dc current.

When the switch S_1 and S_2 is off the inductor discharges and the voltage across the inductor decreases. During the negative half cycle of operation inductor L_3 and L_4 will charge. The diode D_2 and D_4 will be turned on. During the negative cycle of operation, the switch S_1 and S_2 turned on when the inductor charges.

Fig.10 shows the input voltage and current waveforms for inductors. The current flowing through the inductor L1 and L2 is referred to when the input ac voltage is positive. When the cycle is negative the current through the inductor reverses. The amount of circulating current flowing through the inductor L_1 and L_2 is higher com-pared to L_3 and L_4. This can be eliminated by connecting the diode in series with the inductor L_1 and L_2. Small amount of circulating current is flowing in the circuit and this can be reduced by connecting the diode at the supply terminal of the converter. The current flowing through the inductor based on the on and off time of the semiconductor switches. Thus shows there is no overlapping in the operation of the passive components. The charging and discharging of the inductor follows the switching operation and does not affect the operation of capacitor.

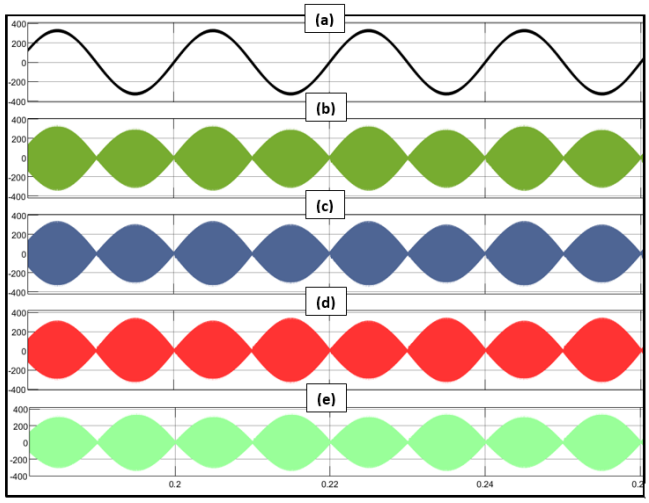

Fig.9. Performance of the inductor voltage. (a) Voltgae acorss the input ar 230 V (rms). (b) The voltage across inductor L_1, (c) L_2, (d) L_3 and (e) L_4

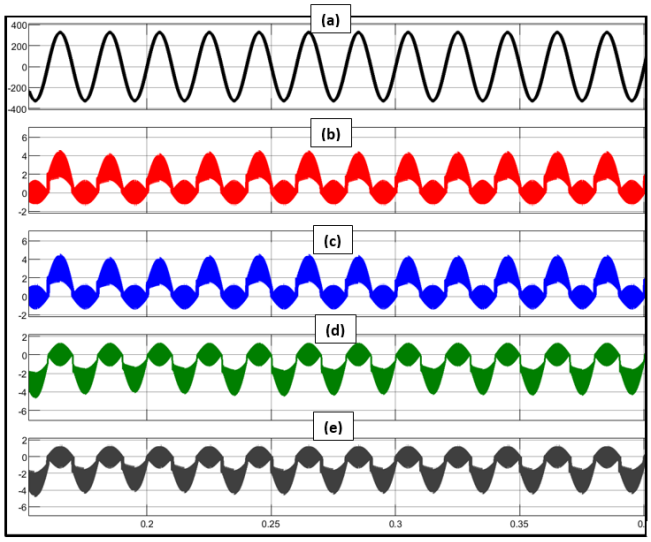

Fig.10. Performance of the inductor current. (a) Voltgae acorss the input ar 230 V (rms). (b) The inductor current in L_1, (c) L_2, (d) L_3 and (e) L_4.

The value of the measured power factor with the nominal supply voltage is provided in Table II. From the table it can be found that the proposed converter can provide high power factor with the wide range of input supply voltage. The power factor of the converter is almost unity at rated voltage.

TABLE II. VOLTAGE, POWER FACTOR AND THD

Input Voltage (in rms)	70	100	150	200	230
Power Factor	0.9994	0.9989	0.9974	0.9954	0.9938
THD (%)	8.2	6.3	5.8	4.1	4.4

The THD of the converter is measured at the input voltage of 70-230 V (rms). The value of the THD is improved at the rated voltage of the converter and measured as 4.8%. However, the value of THD is higher when the input voltage is lower.

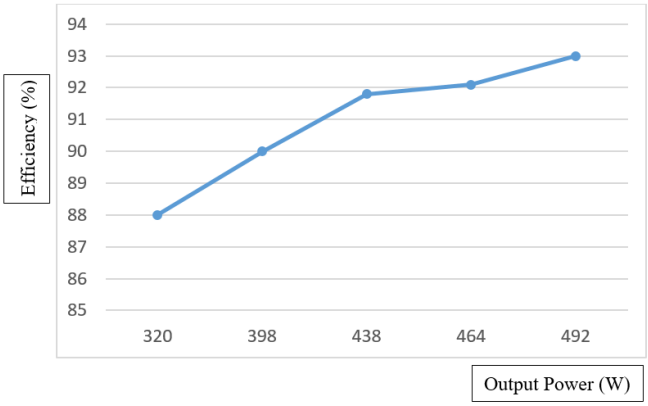

Fig.10. Efficiency of the proposed converter

In Fig 10. the efficiency of the proposed converter is observed as 93 % at the rated voltage of 230 V (rms). When the voltage at the input is lower the efficiency is dropped.

VI. CONCLUSION

This research presents a Two-stage, two phase Interleaved Bridgeless SEPIC based Power Factor Correction Converter for Electric Vehicle Charging Application. The design of the proposed converter is simulated by using MATLAB Simulink software. The proposed PFC converter is simulated with the input supply of 70-230 V, 50 Hz ac supply for 500 W operation. The simple closed loop control circuit is used to generate the signal to turn on the MOSFET with switching frequency of 50kHz. The proposed converter is designed with two MOSFET switches. The pf of the converter is measured for 70 -230 V ac supply. The value of pf is 0.9938 at 230 V input supply and 0.9994 at 70 V input supply. The value of pf is improved compared to other topologies. From the performance of the voltage and current waveforms for the switching devices and the passive components shows that the ripple content is lower and thus decreases the power loss and improve the converter efficiency.

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